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What is Claimed is:

1 1. A dynamic power management device for supplying power
2 to a solid state memory integrated circuit, said device
3 comprising:

4 power control means for supplying a variable
5 voltage to said memory integrated circuit; and

6 logic control means responsive to data access
7 activity for generating address and control signals
8 for said memory integrated circuit and for controlling
9 said power control means to supply power to said
10 memory integrated circuit sufficient to maintain
11 memory information in said memory integrated circuit
12 during periods of no data access activity and
13 sufficient to exchange memory information with said
14 memory integrated circuit during periods of data
15 access activity, whereby power consumption of said
16 memory integrated circuit is curtailed.

1 2. The apparatus of Claim 1, further comprising I/O means
2 for converting parallel data signals to serial data signals
3 for input to said memory integrated circuit and for
4 converting data signals output from said memory integrated
5 circuit from serial to parallel and performing error
6 correction on the resulting parallel data signals.

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1 3. The apparatus of Claim 2 wherein said power control
2 means comprises means for selecting between alternate power
3 sources, a switching regulator, and means for feeding
4 voltage information back to said logic control means.

1 4. The apparatus of Claim 3 wherein said voltage
2 information includes both voltage output information used
3 by said logic control means to cause said power control
4 means to maintain a specified voltage output, and voltage
5 source information used by said logic control means to
6 cause said means for selecting to select one of said
7 alternate power sources.

1 5. The apparatus of Claim 2 wherein said logic means
2 comprises a DMA controller, a data sequencer, and a timing
3 sequencer.

1 6. The apparatus of Claim 5 wherein said logic control
2 means further comprises refresh timer means for timing
3 refresh intervals, a binary address generator, and an
4 encoder, together for generating said address signals for
5 said memory integrated circuit.

1 7. The apparatus of Claim 2 further comprising slew rate
2 controller means for limiting the time rate of change of

3 voltage of said control signals and said data signals input
4 to said memory integrated circuit.

1 8. The apparatus of Claim 2 wherein said logic control
2 means causes said power control means to supply to said
3 memory integrated circuit a relatively low voltage during
4 a standby period, a higher voltage during memory refresh,
5 and a still higher voltage during memory access.

1 9. The apparatus of Claim 2 further comprising daisy
2 chain controller means for enabling communication with
3 another dynamic power management device.

1 10. The apparatus of Claim 2 wherein said logic control
2 means is provided with a sleep mode for conserving power
3 during periods of inactivity.